REMARKS

Claims 1-7 are pending in the application, with Claims 1 and 5 being the independent claims. Claims 1 and 5-7 are rejected under 35 U.S.C. §103(a) as being unpatentable over Khlat (E.P. 0948128 A1) in view of Ratto (US Patent No. 6,993,091). Claim 2 is rejected under 35 U.S.C. §103(a) as being unpatentable over Khlat in view of Ratto in further view of Kataoka et al. (JP 10247953). Claim 4 is rejected under 35 U.S.C. §103(a) as being unpatentable over Khlat in view of Mitama (EP 0863606A1). Claim 3 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all limitations of the base claim and any intervening claims.

Reconsideration of this application is respectfully requested.

On page 5 of the Office Action under "Response to Arguments," the Examiner states, "Applicant's amendment necessitated the new ground(s) of rejection presented in this Office Action." However, the previous Office Action was a 102(b) rejection based on Khlat. Claims 1 and 5 were amended in the reply to the Office Action, the Examiner kept the same format and passages as to Khlat and applied the newly cited art (Ratto) to the added limitation under 103(a). In essence, the arguments presented in the reply to the Office Action were not addressed because Khlat is still kept. Therefore, those same arguments are again presented because they are still relevant due to the presence of Khlat as prior art of record.

The present application recites a direct conversion receiver for substantially removing DC offset to recover an information signal from a carrier signal modulated by the information signal. Adachi, Kataoka and Mitama also recite direct conversion receivers.

In all 35 U.S.C. §103(a) rejections, the Examiner bears the initial burden of factually supporting a prima facie conclusion of obviousness. To establish a prima facie case of obviousness under 35 U.S.C. §103(a) based upon a combination of references, the cited combination of references must disclose, teach or suggest all elements/features/steps of the claim

at issue. All of the claimed features of independent Claims 1 and 5 are not taught or suggested by the combination of *Khlat* and *Ratto* or by either reference alone.

Claim 1 utilizes "means for" recitations, and as such requires the Examiner to consider the specific structure described in the specification to interpret these limitations. In particular, Claim 1 recites a direct-conversion receiver for substantially removing DC offset signals in a mobile communication terminal wherein the receiver comprises, in part, an adjusting means for substantially reducing the difference. Khlat, as cited by the Examiner, takes the output from a low pass filter and subtracts the outputs; thereby providing a means for reducing the difference between the two DC offset components, but does not teach or suggest the specific structure disclosed by the invention, namely the feedback loop circuit **600c**. Khlat instead discloses that the gain/phase correction block **200** may be realized in hardware or software. However, Khlat disclosed a hardware implementation shown in Fig. 2 consisting of a gain adjustment & phase θ correction **200** and complex low pass filter **210**. Khlat discloses that the Ad and θ control signals are factory set, and are intended to remove any phase or gain mismatches occurring between the I and Q paths as a result of analog device variations. The Iout and Qout signals are then filtered by the complex LPF **210** to produce IDCest and QDCest signals representing the DC offset component of the Iout and Qout signals.

In contrast, the feedback loop circuit disclosed by the present invention includes a high gain amplifier **623** for detecting the DC offset component, and an analog-to-digital converter (ADC) **621** for transforming an analog DC offset signal to a digital signal to enable a digital processor (DSP) **619** to read the signal and determine whether the DC offset is zero or not and output a pertinent voltage control voltage to an automatic gain controller to adjust the DC offset signal to zero. The present invention, as claimed, does not read on Khlat because the two implementations differ diametrically. Therefore, the "means for" limitation recited in the invention cannot be broadly interpreted by the Examiner to read on the implementation taught by Khlat. The structure disclosed by the Applicant cannot be disregarded. Ratto does not cure the

deficiencies of Khlat. Because the combination of Khlat and Ratto does not teach or suggest each and every element of Claim 1, it does not render Claim 1 obvious. Accordingly, Claim 1 is erroneously rejected.

Claims 2-4 depend from and contain all the elements of Claim 1. Claims 2-4 are distinguishable from Khlat in the same manner as Claim 1. In addition, paragraph 3 of the Office Action indicates that Claim 2 is rejected under 35 U.S.C. §103(a) as being unpatentable over Khlat in view of Ratto in further view of Kataoka et al. (JP 10247953). However, in the body of the rejection (See page 4) The Examiner states, "However Adachi teaches the following..." It is not clear what the Examiner is referring to. Clarification is respectfully requested.

Furthermore, the Examiner failed to articulate a proper motivation. Instead, the Examiner indicated the result of modifying Khlat by the teachings of (a) Adachi produces one of the methods among many possible methods to generate I and Q components and (b) Kataoka producing the means for fine tuning DC offset cancellation in the receiver. The Examiner articulates the result of modifying the references but fails to explicate why an artisan of ordinary skill in the art would be motivated to perform said modifications. The Examiner's conclusory statement is unaccompanied by evidence or reasoning and is entirely inadequate to support the rejection. *In re Sichert*, 566 F.2d 1154, 1164, 196 USPQ 209, 217 (CCPA 1977). Accordingly, the Examiner fails to meet the requirements set forth in MPEP §706.02(j).

Moreover, in rejecting Claim 4 the motivation as articulated by the Examiner is hopelessly deficient. The Examiner asserted: "Thus, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the combination to provide the following: a switching means for connecting the converting means to detecting means as this arrangement would provide alternative method for implementing DC offset cancellation in a receiver as taught by Mitama." Once again, the Examiner articulates the result of modifying the reference but fails to explicate why an artisan of ordinary skill in the art would be motivated to perform said modifications. Once more, the Examiner fails to meet the requirements set forth in MPEP §706.02(j).

Regarding independent Claim 5, the Examiner states that *Khlat* discloses all of the elements of Claim 5 except for "determining whether DC offset is zero and outputting a control voltage to adjust DC-offset to zero," which the Examiner states is disclosed by Ratto. Applicant respectfully disagrees. The Examiner cites col. 3, lines 10-31 in support of the rejection. Ratto teaches means for determining the DC-offset caused by the I/Q modulator on the basis of the test vectors and the feedback vectors caused by the test vectors and being comprised of the I- and Q-feedback signals, and means for determining the correction parameters of DC-offset on the basis of the determined DC-offset. (See col. 3, lines 24-29).

The "broadest reasonable interpretation" that an Examiner may give means-plus-function language is that statutorily mandated in paragraph six. Accordingly, the PTO may not disregard the structure disclosed in the specification corresponding to such language when rendering a patentability determination. (See MPEP § 2181, Rev. 5,Aug. 2006).

Ratto discloses the determination step as follows. "According to the preferred embodiment of the invention, two test vectors T1 and T2 are used, the vectors being equal in their absolute value but opposite in their phases, i.e.T1=T2. The amplifier 8 is then retained in the linear operation range, in which case it does not distort the test signal traveling therethrough." (See col. 5, lines 18-23).

In contrast, the determination step disclosed by the present invention includes a high gain amplifier **623** for detecting the DC offset component, an analog-to-digital converter (ADC) **621** for transforming an analog DC offset signal to a digital signal to enable a digital processor (DSP) **619** to read the signal and determine whether the DC offset is zero or not and output a pertinent voltage control voltage to an automatic gain controller to adjust the DC offset signal to zero. Consequently, Ratto does not cure the deficiency of Khlat, because the "broadest reasonable interpretation" that an Examiner may give the means-plus-function language recited in Ratto is the structure disclosed in the specification corresponding to such language. The structure disclosed by Ratto is to use "two test vectors T1 and T2, the vectors being equal in their absolute

value but opposite in their phases." Because Ratto fails to cure Khlat's deficiency, the combination does not teach or suggest each and every element of Claim 5. The Examiner, therefore, fails to make a prima case of obviousness as to Claim 5.

Claims 6-7 depend from and contain all the elements of Claim 5. Claims 6-7 are distinguishable from Khlat and Ratto in the same manner as Claim 5.

The application as now presented, containing Claims 1-7 are believed to be in condition for allowance. Should the Examiner believe that a telephone conference or personal interview would facilitate resolution of any remaining matters, the Examiner may contact Applicant's attorney at the number given below.

Respectfully submitted,

Michael J. Musella
Reg. No. 39,310
Attorney for Applicants

THE FARRELL LAW FIRM, PC
333 Earle Ovington Boulevard, Suite 702
Uniondale, New York 11553
TEL: (516) 228-3565

MJM/EC/mk